# Short Papers

## Cryogenically Cooled GaAs FET Amplifier with a Noise Temperature Under 70 K at 5.0 GHz

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*Abstract*—**A 4.5–5.0-GHz gallium arsenide field-effect transistor (GaAs FET) amplifier cryogenically cooled to approximately 70 K is described. A noise temperature of under 70 K is achieved over the band. Power gain for the two-stage amplifier is 20 dB. A noise analysis is performed to predict noise-temperature dependence on the temperature of the amplifier.**

### Introduction

The GaAs FET is presently one of the most attractive devices available to the designer of low-noise microwave amplifiers. A rapid succession of improvements in fabrication technology and device design has resulted in reliable devices that can be produced in quantity with noise and gain performance that would have been viewed as incredible several years ago. Uses for FET's are not restricted to low-noise amplifiers. They have shown great potential as high-power amplifiers, oscillators, mixers, and switches [1].

Since most of the noise generated by the FET is thermal, a substantial noise figure reduction may be realized if one simply cools the device. Unlike the bipolar transistor, whose gain drops with decreasing temperature, the FET gain increases, producing the desirable effect of further enhancing its output signal-to-noise ratio (SNR) for a given fixed input SNR. Here it is manifesting an ideal combination of properties.

This short paper describes a two-stage single-ended GaAs FET amplifier cryogenically cooled to 70 K designed to cover the 4.5–5.0-GHz range. Its purpose is to serve as a low-noise second stage to a parametric amplifier in a radio astronomy receiver. The amplifier has a nominal gain of 20 dB at the cold temperature and a noise temperature under 70 K over the full band.

In an effort to acquire an ability to predict (albeit roughly) the noise temperature at the cold temperature and to gain some insight into the mechanisms which are responsible for the noise-temperature improvement, an analysis of a rather simplified GaAs FET noise model was performed. Key results of this work are presented. The model's validity is restricted but is useful when the device is biased at the point of minimum noise figure.

To corroborate the analysis, single-stage amplifier noise-temperature measurements were made and presented here.

### Amplifier Description

The amplifier utilizes microstrip circuitry etched on 25-mil-thick alumina. The GaAs FET is the NE 244. $S$-parameter and two-port noise parameter measurements were made at 300 K and provided the basis for the design. The $S$ parameters and optimum generator reflection coefficient are presented in Table I. As shown in [2], $S_{11}$, $S_{22}$, and $S_{12}$ are practically invariant with temperature in this frequency range. The forward transducer gain, $|S_{21}|^2$, is strongly dependent on temperature, however. Insight into the $S_{21}$ dependence may be acquired by investigating the low-frequency transconductance $g_m$ variation with temperature since $|S_{21}|$ is proportional to $g_m$. We show in the next section that the transconductance is approximately proportional to $T^{-1/2}$ from 70 to 300 K.

TABLE I
MEASURED $S$ PARAMETERS AND OPTIMUM GENERATOR REFLECTION COEFFICIENT

| Freq. (GHz) | $S_{11}/\theta$ | $S_{21}/\theta$ | $S_{12}/\theta$ | $S_{22}/\theta$ | $\Gamma_{opt}$ |
|---|---|---|---|---|---|
| 4.0 | .94/-57 | 1.58/116 | .009/52 | .92/-31 | - |
| 4.5 | .92/-63.5 | 1.44/109 | .006/180 | .90/-32.5 | .7/+90 |
| 5.0 | .90/-71 | 1.33/97 | .005/161 | .87/-41.5 | .7/+100° |
| 5.5 | .86/-79 | 1.30/83.5 | .006/142 | .83/-48 | - |

*Note:* $V_{DS}$ = 3.0 V; $I_D$ = 10 mA; $T_{AMB}$ = 300 K.

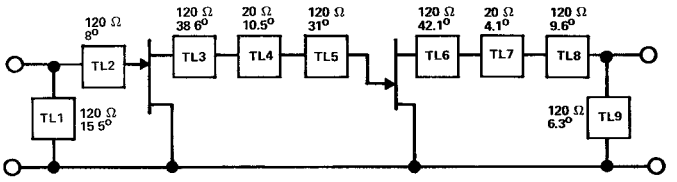


Fig. 1. Circuit configuration. All degrees referred to 4.7 GHz.

Input, interstage, and output matching networks were designed using the room-temperature transistor data and Smith chart matching techniques. The final values of the network elements were arrived at with the aid of computer optimization. The final circuit appears in Fig. 1.

The input and output impedances are of necessity different from 50 Ω. Voltage standing wave ratios (VSWR's) of 4:1 to 7:1 are generally measured with GaAs FET amplifiers in this frequency range. The high VSWR's are a result of noise match and stability requirements. High output VSWR's are also a consequence of the shortcomings of realizable practical matching networks. To obviate these drawbacks, two cryogenic isolators were integrated with the amplifier so that the input/output VSWR's would be under 1.3:1.

A severe problem is destructive stresses that develop at electrical connections at the cold temperature due to the dissimilar coefficients of contraction of the various materials and components which comprise the complete amplifier. Since the matching networks are of the distributed type, realized in microstrip, they presented no problem. Attention was focused on the bias resistors and bypass capacitors. We chose chip resistors that utilized a resistance element deposited on an alumina substrate. The capacitors were made of a ceramic material—not alumina—whose coefficient of contraction seems to be very similar to alumina. Strain reliefs at the input and output connections were incorporated to alleviate the stress at these points. It is important to allow adequate clearance between the amplifier housing, which is typically aluminum, and the substrate. Aluminum contracts four times as much as alumina. Inadequate

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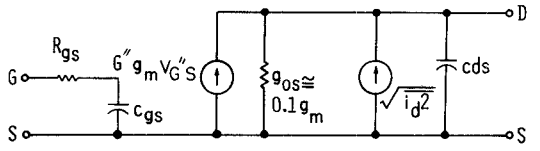


Fig. 2. GaAs MESFET noise model.

clearance at room temperature could result in a fractured substrate at the cold temperature.

Proper heat sinking of the transistors was necessary to ensure that the transistor would be cooled to nearly the same temperature as the amplifier housing. Of concern are the transistor-substrate thermal path and substrate-housing thermal path. By soldering the NE 24406 package carrier to the substrate's ground plane, we reduced the thermal resistance of this path to an absolute minimum. The thermal resistance of the NE 24406 with this mounting arrangement is conservatively estimated to be 50°C/W. At minimum noise figure bias, the device is dissipating about 30 mW. Therefore, the channel temperature is at most 2° higher than the substrate temperature. To minimize the thermal resistance of the substrate-housing interface, two measures were taken. We selected a substrate for flatness and machined the shelf on which it is placed extremely flat. The surface finish of the shelf was on the order of 0.1 mil. To further guarantee uniform contact, a 2-mil sheet of indium was placed between the substrate and the housing.

## Noise Analysis Model and Key Results

Far more rigorous and thorough noise analyses of the GaAs FET appear in the literature, but they tend to yield equations that cannot easily be applied unless the user first determines a host of constants and parameters for his particular device. Secondly, none has, to the author's knowledge, given sufficient emphasis to the temperature dependence of GaAs FET noise figure to the point of generating user-oriented practical results.

The simplified model (Fig. 2) analyzed here emphasizes the important role the low-frequency transconductance $g_m$ plays in the noise temperature of the device and the effects of impedance matching and physical temperature on its "noisiness." For this simple model, therefore, the gate noise generator of van der Ziel [3], the thermal noise generators corresponding to the source and gate contact resistances, the interelectrode capacitances, and source inductances have been neglected.

After van der Ziel [3] we assumed the channel noise to be represented by a noise generator of the form

$$\overline{id^2} = K_c K T_{\mathrm{FET}} g_m \Delta f, \qquad K_c = 2.4$$

with the usual meanings attached to the various quantities. As pointed out [4] this model is valid only when the mobility of the majority carriers in the channel is constant. At low bias currents ($I_D \approx 0.2 I_{DSS}$) where minimum noise figure typically occurs, the assumption of constant mobility is a valid one.

We calculated the noise figure of the amplifier illustrated in Fig. 3 using the basic definition of noise figure $F$, i.e.,

$$F = \frac{\left(\frac{S_i}{N_i}\right)}{\left(\frac{S_0}{N_0}\right)}.$$

The symbols are defined in Fig. 3.

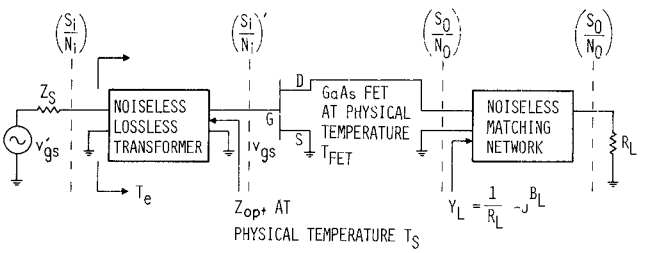


Fig. 3. Single-stage amplifier with definition of symbols for noise calculation.

The transconductance is a function of transistor operating point and its physical temperature through its dependence on mobility, and the mobility of the majority carriers in the channel is a function of temperature. For physical temperatures greater than approximately 60 K, the mobility may be described by

$$a(T_{\mathrm{FET}})^x$$

where $a$ is a constant and the exponent $x$ assumes a range of values depending on the material and doping level. Curves for the mobility of charge carriers in a doped semiconductor appear in the literature [5]. A frequently used value for the exponent is $-3/2$. From measurements made on actual transistors at AIL over the temperature range of 300–70 K and from [6], it appears that the exponent is closer to $-1/2$. The lower exponent is due to velocity saturation of the carriers in the channel. The mobility for a typical semiconductor is maximum at about 60 K and decreases below 60 K because impurity scattering comes into play.

By postulating a function for the transconductance $g_m$ of the form $K(T_{\mathrm{FET}})^{-1/2}$ where $T_{\mathrm{FET}}$ is the physical temperature of the GaAs FET, we get the following result for the noise temperature $T_e$ of the GaAs FET:

$$T_e = 290 \left(\frac{0.6}{g_m R'}\right) \times \left(\frac{T_{\mathrm{FET}}}{T_s}\right)^{3/2} \tag{1}$$

where $g_m$ is the low-frequency transconductance at temperature $T_s$ (300 K, for convenience), and $R'$ is given by

$$\frac{R_s \left|1 - \left(\frac{R_s}{R_s + j\omega L_1}\right)\right|^2}{\omega^2 C_{gs}{}^2 |Q|^2}$$

where

- $\omega$ radian frequency, radians per second;
- $R_s$ 50 Ω;
- $C_{gs}$ gate-source capacitance of FET;
- $|Q|^2 = |Z_{\mathrm{opt}} + Z_{\mathrm{in}}|^2$;
- $Z_{\mathrm{in}}$ input impedance of FET;
- $Z_{\mathrm{opt}}$ optimum source impedance for minimum noise temperature.

At 4.7 GHz, $R'$ is calculated to be approximately 15 Ω. The transconductance $g_m$ is 26.5 mmho and $T_s$ is 300 K. The reactance $j\omega L_1$ is the lumped-element equivalent reactance of the shorted stub $TL1$ in the input matching network (Fig. 1). The equation for $T_e$ is plotted in Fig. 4 as a function of $T_{\mathrm{FET}}$.

## Noise-Temperature Measurements

Noise-temperature measurements on the single-stage 10-dB FET amplifier were performed using an AIL 20 K parametric amplifier having 15-dB gain as the second stage. With this con-

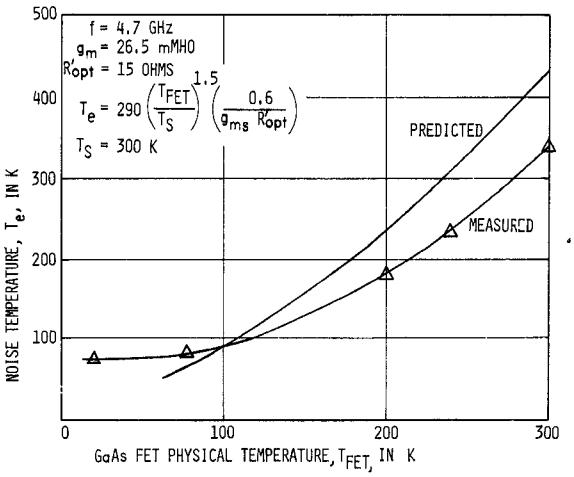


Fig. 4. GaAs FET amplifier noise temperature.

figuration, the second-stage contribution in the noise-temperature measurements was no more than 10 K.

Noise-temperature measurements on the 20-dB FET amplifier were made with an AIL precision receiver and mixer–preamplifier as the second stage. The total correction to the noise-temperature measurement was on the order of 30 K.

The noise source for the preceding measurements was the AIL 7009 hot/cold noise generator.

## Discussion of Results

The single-stage and two-stage amplifiers required little alignment at room temperature to get the desired performance. Adjustment of biases was all that was required. The single-stage amplifier had 8.5 ± 0.2-dB gain and a noise figure of 3.5 dB maximum over the band. The two-stage unit had 16 dB of gain at midband with a gain tilt of about −3 dB/500 MHz. Its noise figure was 2.6 dB maximum. The lower noise figure was achieved through transistor selection.

The gain tilt associated with the two-stage unit at first seemed undesirable but later proved to be an advantage. The intended application for this unit is to serve as a second stage to a cooled paramp. By introducing an opposite gain tilt in the paramp through a slight bias adjustment, we achieve a flat overall gain response. Since the paramp is called on to provide 3 dB more gain at the upper band edge, the noise contribution of the FET to the overall paramp FET noise temperature is cut in half. This measure provides a nearly flat noise temperature for the combination.

The units were installed in a liquid helium refrigerator equipped with 70 and 20 K stations. Cool-down time was approximately 3–4 h for the units.

The passband of the single-stage unit tended to skew as the temperature was lowered. The single-stage unit was required to have a gain flatness of 0.5 dB peak to peak from 4.5 to 5.0 GHz at 20 K. To achieve this flatness, the output matching network was retuned to introduce an opposite tilt at room temperature. At each temperature of interest the gate bias was adjusted for minimum noise figure, which coincidentally was also the point of maximum gain. We observed that the gate bias had to be steadily increased as the temperature was lowered. The explanation for this is that since the saturation current $I_{DSS}$ and the pinchoff voltage $V_p$ are increasing with decreasing temperature, larger negative gate bias is required so that the drain current $I_D$ could be held to 20 percent of the saturation

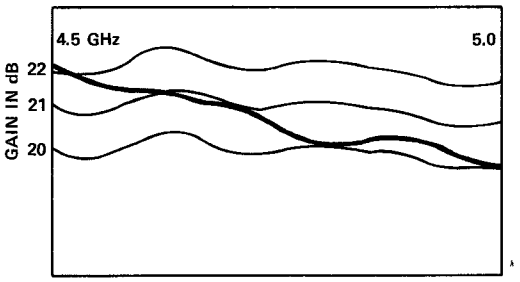


Fig. 5. Gain response of two-stage GaAs FET amplifier.

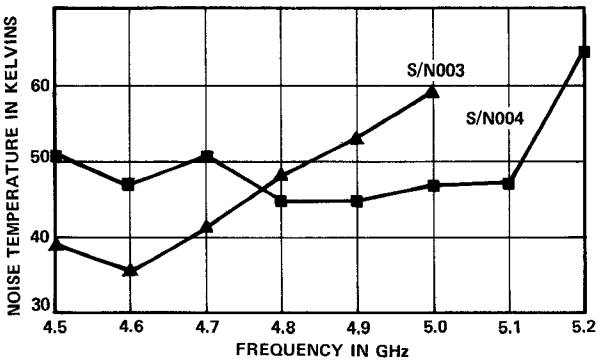


Fig. 6. Noise temperature of two-stage GaAs FET amplifier.

drain current. This is the point of minimum noise figure in the GaAs MESFET. It is the point at which diffusion noise is insignificant.

We performed similar bias adjustment on the two-stage unit to achieve minimum noise figure. The tilt we observed at room temperature was still present at 70 K but smaller by 1 dB.

In Fig. 4 the noise temperature predicted by analysis is plotted along with the measured amplifier noise-temperature data. Although the variation seems to follow the actual variation of noise temperature, it would seem plausible to expect the predicted noise temperature to be perhaps 30 to 50 percent lower than the measured data since we have neglected the gate current and contact resistance noise generators. It is not and this may be so for several reasons. Foremost among them may be that the actual value of $K_c$, assumed to be 2.4, may be considerably lower than that value. Secondly, as explained in [4] there exists a strong correlation (almost unity) between the drain noise and induced gate noise, which leads to a high degree of cancellation in the noise output of the GaAs FET. Since we have omitted the gate noise generator, it seems plausible that the noise temperature of the FET as predicted from the analysis would be pessimistic in spite of the fact that the contact resistance noise generators were omitted.

Fig. 5 depicts the gain response of the 20-dB GaAs FET amplifier cooled to approximately 70 K, and Fig. 6 is a plot of noise temperature over the 4.5–5.0-GHz band. The amplifier noise temperature is well under 70 K. Preliminary results from a production run indicate that this performance is rather typical for the units and is in no way unusual.

With a paramp cooled to 20 K preceding the two-stage FET amplifier, we have reliably and repeatedly achieved noise temperatures under 16 K over the band. The overall gain of the combination was 36 dB.

The output power at the 1-dB compression point was well in excess of +5 dBm for the FET amplifiers. Input/output VSWR's were well below 1.3:1.

## Conclusion

Data show that it is presently feasible to construct low-noise GaAs FET amplifiers with performance comparable to uncooled parametric amplifiers. They exhibit the qualities of easy alignment, require little testing time, and demonstrate a high degree of gain stability. Saturation powers well in excess of those associated with parametric amplifiers are easily attained. The simplicity of the approach makes the cooled GaAs FET amplifier an attractive candidate as a second stage to a parametric amplifier. Using 1/2-$\mu$m GaAs FET's, it should be possible to realize noise temperatures well under 40 K in this frequency range.

The first-order analysis presented in this short paper for a simplified noise model of the FET yields results that correlate well with measurements.

## Acknowledgment

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# A Quasi-Linear Approach to the Design of Microwave Transistor Power Amplifiers

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***Abstract*—A method of large-signal transistor characterization and power amplifier design is described which allows the designer to predict the load and source terminations required for optimum added-power circuit efficiency, and to see graphically how efficiency and power gain change as a function of the load termination. Experimental results obtained with a 1-W bipolar junction transistor (BJT) amplifier at 1.3 GHz are presented.**

## Introduction

It is well known that microwave transistor power amplifiers are currently designed by largely empirical techniques [1], [2] since a suitable analytic approach has not been available. Perhaps one of the most successful large-signal design techniques to date has been the automatic load contour approach reported by Cusack *et al.* [3]. This technique is basically an automated version of the more conventional cut-and-try experimental approach to power amplifier optimization. Some limited success with a large-signal $S$-parameter characterization has also been reported [4]. In this short paper an analytic design approach is presented which is based upon a large-signal $y$-parameter characterization of high-frequency bipolar junction transistors (BJT's).

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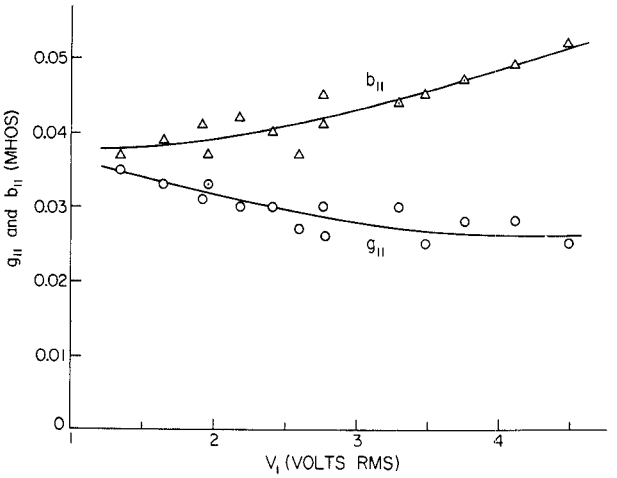


Fig. 1. Measured large-signal values of $y_{11}$ for the CTC D1-28Z transistor at 1.3 GHz under fixed-bias conditions. $V_{CC}$ = 20 V; $I_C$ = 100 mA.

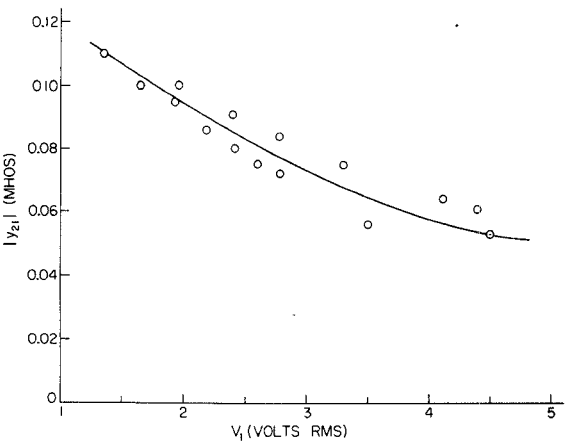


Fig. 2. Measured large-signal values of $|y_{21}|$ for the CTC D1-28Z transistor at 1.3 GHz under fixed-bias conditions. $V_{CC}$ = 20 V; $I_C$ = 100 mA. The angle of $y_{21}$ remains constant at $-175°$.

## Large-Signal $Y$-Parameter Characterization

In 1970, Houselander *et al.* [5] proposed that the large-signal behavior of a BJT in common-base or common-emitter configuration could be approximately characterized by a set of large-signal $y$ parameters. In this characterization, $y_{11}$ and $y_{21}$ were considered to be functions of the input RF voltage $V_1$, while $y_{12}$ and $y_{22}$ were considered to be constant. The parameters $y_{11}$ and $y_{21}$ are most closely identified with the forward-biased base-emitter junction of the BJT, while the parameters $y_{12}$ and $y_{22}$ are most closely identified with the reverse-biased base-collector junction. Hence one would anticipate that most of the nonlinearity would be associated with the parameters $y_{11}$ and $y_{21}$, provided that significant clipping does not occur at the output of the transistor. This assumption of no significant clipping at the output of the BJT appears to be valid in high-frequency operation. A good discussion of this approach to the large-signal characterization of a high-frequency BJT may be found in Spence [6].

For this investigation, measurements were made of the large-signal $y$ parameters of a silicon BJT rated at 1-W output at 960 MHz (CTC D1-28Z) using a measurement technique described in [7]. Figs. 1–4 show the measured results for a typical device at 1.3 GHz when biased to $V_{CC}$ = 20 V, $I_C$ = 100 mA.